REMARKS

Claims 1-7, 15-26, and 30-35 are pending. Claims 1, 15, and 19 are in independent form.

In the Office action mailed September 19, 2007, the Examiner noted that the status identifier for claim 19 in the response filed July 9, 2007 was in error.

Applicant thanks the Examiner, not only for recognizing the error, but also for the courtesy of advancing prosecution notwithstanding the error. Applicant will endeavor to ensure that such errors do not occur again.

Claim 12 was rejected under 35 U.S.C. § 112, second paragraph, as indefinite. The rejection is allegedly based on a failure to establish antecedent basis for "the single write line."

Applicant respectfully traverses the rejection. As a threshold matter, claim 12 was canceled prior to the Office action mailed September 19, 2007. As for claim 35, which recites "the single write line," parent claim 15 recites an effective write port that includes "a single write line to write to addresses in different banks..."

Accordingly, antecedent basis for the recitation of "the single write line" in claim 35 has been established. Applicant respectfully requests that the rejection under 35 U.S.C. § 112, second paragraph, be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claim 1 was rejected under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,933,627 to Parady (hereinafter "Parady") and U.S. Patent No. 5,787,454 to Rohlman (hereinafter "Rohlman").

Claim 1 relates to an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, and a general purpose register set to store and obtain operands for the arithmetic logic unit.

The register set includes a plurality of two-ported random access memory devices assembled into banks. The register set includes two effective read ports and one effective write port. The effective write port includes write ports of a pair of the two-ported random access memory devices. Each bank is capable of performing a read and a write to two different words in the

same processor cycle. The arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port.

The rejection of claim 1 contends that Rohlman's memory cells form memory banks, as recited. *See office action mailed September 19, 2007*, page 4, para. 10 (describing that "for purposes of the rejection, Rohlman's memory cells are equated to the claimed memory bank, since Rohlman's memory cells meet the claimed meaning on memory bank.").

Applicant respectfully disagrees. In this regard, attention is respectfully directed to FIG. 6, which shows Rohlman's memory cell and is now reproduced for the sake of convenience. *See, e.g., Rohlman*, col. 2, line 66-67.

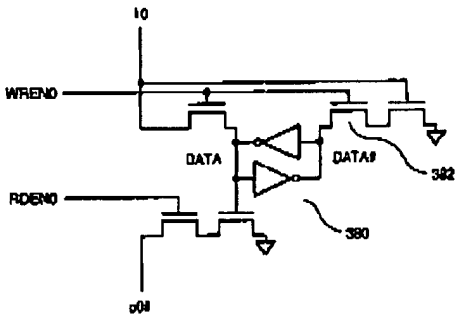

FIG. 6

According to Rohlman, *each memory cell stores one bit of data. See, e.g., id.*, col. 1, line 13-14. Moreover, each memory cell has only one write enable (wren0) and one read enable (rden0).

See, e.g., id., col. 6, line 45-47. The write enable allows storage of the data input i0 to cell 380. *See, e.g., id.*, col. 6, line 47-48. The read enable allows the data stored in cell 380 to be read from the data output o0. *See, e.g., id.*, col. 6, line 50-52.

Since Rohlman's cells each are capable of storing a single bit, reading a single bit, and writing a single bit, Rohlman's cells are not capable of performing a read and a write to two different words, much less two different words in a same processor cycle, as recited of each bank in claim 1. Indeed, there is nothing in Rohlman that describes or suggests how to assemble Rohlman's cells into the recited banks.

Although the rejection does not contend otherwise, please note that the banks in Rohlman's Re-Order Buffer (ROB) also do not constitute the recited banks. In this regard, Rohlman makes it clear that each data input 412, 414, 416, 418 allows data input to a single bank. *See, e.g., id.*, col. 7, line 20-29. None of data inputs 412, 414, 416, 418 can be used to write to each of the multiple banks in Rohlman's Re-Order Buffer (ROB).

Paraday does nothing to remedy these deficiencies in Rohlman. As discussed previously, Paraday is silent as to the architecture of integer registers 48. Parady thus also fails to describe or suggest that two-ported random access memory devices be assembled into the recited banks.

Thus, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 1 is not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 1, and the claims dependent therefrom, be withdrawn.

Claim 15 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Rohlman.

Claim 15 relates to a method for executing multiple context threads. The method includes processing data for executing threads within an arithmetic logic unit, operating control logic to control the arithmetic logic unit, and storing and obtaining operands for the arithmetic logic unit within a general purpose register set comprising a plurality of banks of two-ported random access memory devices.

The register set includes two effective read ports and one effective write port. The effective write port comprises write ports of a pair of the two-ported random access memory devices. The effective write port includes a single write line to write

to addresses in different banks of the plurality of banks. Each bank is capable of performing a read and a write to two different words in the same processor cycle.

The rejection of claim 15 also contends that Rohlman's memory cells form memory banks, as recited.

Applicant respectfully disagrees. As discussed above, Rohlman's cells each are capable of storing a single bit, reading a single bit, and writing a single bit. Rohlman's cells are not capable of performing a read and a write to two different words, much less two different words in a same processor cycle, as recited of each bank in claim 15. Indeed, there is nothing in Rohlman that describes or suggests how to assemble Rohlman's cells into the recited banks.

Paraday does nothing to remedy these deficiencies in Rohlman. As discussed above, Paraday is silent as to the architecture of integer registers 48. Parady thus also fails to describe or suggest that two-ported random access memory devices be assembled into the recited banks.

Thus, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 15 is not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 15, and the claims dependent therefrom, be withdrawn.

Claim 19 was rejected under 35 U.S.C. § 103(a) as obvious over Parady and Rohlman.

Claim 19 relates to a processor unit that includes an execution unit for execution of multiple context threads. The execution unit includes an arithmetic logic unit to process data for executing threads, control logic to control the operation of the arithmetic logic unit, a general purpose register set to store and obtain operands for the arithmetic logic unit, and a data link between the arithmetic logic unit and the one effective write port of the general purpose register set.

The register set includes a plurality of two-ported random access memory devices. The register set comprising two effective read ports and one effective write port. The effective write port comprises write ports of a pair of the two-ported random access memory devices. The data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port.

The rejection of claim 15 also contends that Rohlman's memory cells form memory banks. *See office action mailed September 19, 2007*, page 7, para. 21 (describing that "for purposes of the rejection, Rohlman's memory cells are equated to

the claimed memory bank, since Rohlman's memory cells meet the claimed meaning on memory bank.").

As a threshold matter, applicant would like to point out that claim 15 does not recite memory banks. Since 35 U.S.C. § 132 and 37 C.F.R. § 1.104(2) both require that the reasons for any adverse action be stated in an Office action, the rejection is facially deficient and Applicant requests that it be withdrawn.

Moreover, neither Rohlman's memory cells nor the banks in Rohlman's Re-Order Buffer (ROB) describes or suggests a register set that includes a plurality of two-ported random access memory devices and that comprises two effective read ports and one effective write port, as recited in claim 19. In this regard, Rohlman's individual memory cells have a single bit and hence do not include a plurality of two-ported random access memory devices, as recited.

As for the banks in Rohlman's Re-Order Buffer (ROB), Rohlman's memory array provides one data output from each memory bank. See, e.g., id., col. 7, line 56-57. Accordingly, the banks in Rohlman's Re-Order Buffer (ROB) are not a register set that comprises two effective read ports, as recited.

Paraday does nothing to remedy these deficiencies in Rohlman. As discussed above, Paraday is silent as to the architecture of integer registers 48. Parady thus also fails to describe or suggest a register set that includes a plurality of two-ported random access memory devices and that comprises two effective read ports and one effective write port.

Thus, even if Paraday and Rohlman were combined, one of ordinary skill would not arrive at the recited subject matter. Accordingly, claim 19 is not obvious over Paraday and Rohlman. Applicant respectfully requests that the rejections of claim 19, and the claims dependent therefrom, be withdrawn.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Attorney's Docket No.: 10559-317001/P9678
Intel Corporation

Applicant asks that all claims be allowed. No fees are believed due at this time. Please apply any charges or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

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